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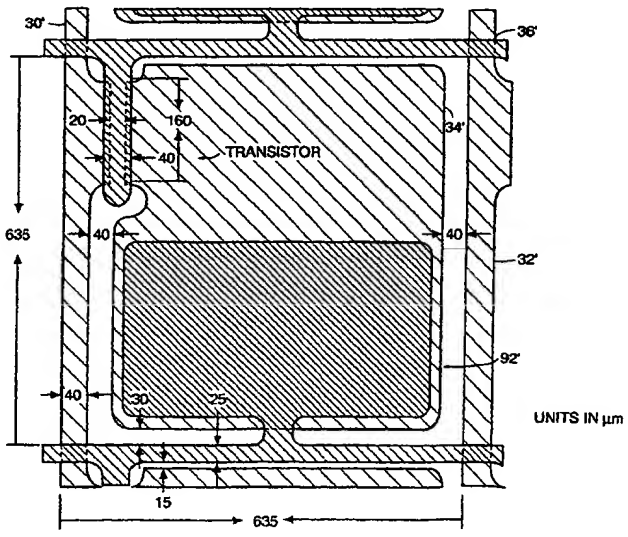

(57) Abstract: A system and method of use of a storage capacitor to improve the appearance and addressing characteristics of an electronically driven display. The capacitor is formed by the overlap of portions of electrodes used to address different pixels, or by the overlap of an addressing line and a conductor. An insulator layer situated between the capacitor electrodes can be the same insulator layer present in an FET transistor used to address the pixel. Methods of use of capacitors to achieve improved display addressing are disclosed.

WO 01/07961 A1

USE OF A STORAGE CAPACITOR TO ENHANCE THE PERFORMANCE OF AN ACTIVE MATRIX DRIVEN ELECTRONIC DISPLAY

Cross Reference to Related Applications

This application claims the benefit of U.S. provisional patent application serial number 60/144,911, filed July 21, 1999, which application is incorporated herein in its entirety by reference.

Field of the Invention

This invention relates generally to systems and methods for addressing an electronic display. More particularly, the invention relates to designs for active matrix backplanes that use a capacitor at each pixel electrode for driving an electronic display.

Background

In an active matrix display, to address a pixel, a voltage is delivered to a pixel by addressing the gate (or select) line for that pixel as well as applying a voltage on the data line for that pixel. The pixel is charged up to a voltage approaching the corresponding data line voltage. After addressing the pixel, the voltage decays due to leakage through the pixel as well as through the thin-film transistor attached to the pixel. Therefore, the pixel does not experience the full voltage drop across its thickness for the entire time between addressing events. In fact, the voltage across the pixel may drop quite considerably between addressing events. This is undesirable because the optical response of the electro-optical medium is slower when the time-average voltage across the pixel is smaller. Also, the optical saturation will generally be smaller when the time-averaged voltage across the pixel is reduced.

Summary of the Invention

In one aspect, the invention features an electronic display that comprises an encapsulated display medium comprising a plurality of pixels. The electronic display includes a transistor having a data electrode, a gate electrode and a pixel electrode and comprising a layer of insulating material situated between a first layer of conductive material that forms the gate electrode and a second layer of conductive material that forms the data and pixel electrodes. The data and pixel electrodes form the source and drain of the transistor. With field-effect transistors

(FETs), either the source or the drain may be connected to the pixel, although typically it is the transistor source which is connected to the pixel. The transistor applies an addressing voltage to one of the pixels via the transistor pixel electrode. The electronic display includes a storage capacitor comprising a layer of insulating material situated between a first layer of conductive material and a second layer of conductive material. The storage capacitor is in electrical communication with the pixel addressed by the transistor for reducing a rate of voltage decay across the pixel. The encapsulated display medium can include electrophoretic particles or needles dispersed in a fluid, or can be bichromal spheres.

In one embodiment, one of the layers of material comprising the transistor and a respective layer of material comprising the storage capacitor comprise a continuous layer of material. In another embodiment, one of the conductors making up the storage capacitor is in electrical communication with a gate line electrode that is not used to address the pixel associated with the storage capacitor, but is adjacent to the pixel. In another embodiment, the storage capacitor is in electrical communication with a conductor that is not connected to any of the gate or data lines. This conductor could be held at a fixed voltage or electronically tied to the front (common plane) electrode of the display.

In one embodiment, the storage capacitor comprises a storage capacitor pixel electrode, an insulator disposed adjacent the pixel electrode and a storage capacitor gate electrode disposed adjacent the insulator. The insulator can be patterned. Alternatively, the insulator is unpatterned.

In one embodiment, the storage capacitor comprises a pixel electrode, an insulator disposed adjacent the pixel electrode and a gate electrode disposed adjacent the insulator. In one embodiment, the storage capacitor comprises a pixel electrode, a semiconductor disposed adjacent the pixel electrode, an insulator disposed adjacent the semiconductor, and a gate electrode disposed adjacent the insulator. In another embodiment, the storage capacitor comprises a pixel electrode, an insulator disposed adjacent the pixel electrode and a conductor disposed adjacent the insulator. In still another embodiment, the insulator forms a part of the storage capacitor and the transistor.

In one embodiment, a capacitance of the storage capacitor is greater than a capacitance of the pixel. In another embodiment, the voltage decay time across the pixel is approximately given

by the product of R_p and (C_p+C_s) where R_p is the resistance of the pixel, C_p is the capacitance of the pixel, and C_s is the capacitance of the storage capacitor.

In another embodiment, the transistor and the storage capacitor comprise a plurality of continuous layers of material.

In a further embodiment, the transistor and the storage capacitor each further comprise a layer of semiconducting material situated between the respective first layers of conductive material and the respective second layers of conductive material.

In another aspect, the invention relates to an electronic display comprising an encapsulated display medium comprising a plurality of pixels, in which each of the pixels comprises at least one capsule containing particles dispersed in a fluid. The electronic display includes a storage capacitor comprising a layer of insulating material situated between a first layer of conductive material and a second layer of conductive material. The storage capacitor is in electrical communication with one of the plurality of pixels for reducing a rate of voltage decay across the pixel.

In still another aspect, the invention relates to a method of addressing an electronic display having a display medium comprising a plurality of pixels and a plurality of storage capacitors, with at least one of the plurality of storage capacitors in electrical communication with a corresponding one of the plurality of pixels. The method comprises applying an electrical pulse to the capacitor to charge the capacitor to an addressing voltage of the corresponding pixel, the duration of the electrical pulse being insufficient in length to fully address the pixel directly, so that the pixel is addressed and presents an intended appearance after the voltage pulse ends. In one embodiment, a plurality of electrical pulses are successively applied to a plurality of capacitors, each pulse charging the respective capacitor to an addressing voltage of the corresponding pixel. In this embodiment, an individual duration of an electrical pulse is insufficient in length to fully address a pixel directly, so that the pixels are addressed and present an intended image after the voltage pulses end, with the total duration of the plurality of pulses being less than an addressing time of the electronic display.

Brief Description of the Drawings

The objects and features of the invention can be better understood with reference to the drawings described below. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention.

FIG. 1 is a plan view of one exemplary embodiment of the circuitry used in addressing a pixel according to principles of the invention.

FIG. 2A-2D are elevation views of a number of illustrative embodiments of the invention.

FIG. 3A-3B are schematic circuit diagrams depicting various exemplary embodiments of the invention.

FIG. 4A shows a plan (or top) view of an embodiment of a thin-film transistor.

FIG. 4B shows a diagrammatic cross sectional view that corresponds to the transistor embodiment shown in FIG. 4A.

FIG. 5 shows a graph of drain current versus gate voltage for a sample of a two-mask transistor of the type shown in FIG. 4A.

FIG. 6A shows a diagrammatic cross-sectional view of an electronic display according to one embodiment of the present invention.

FIG. 6B shows a diagrammatic cross-sectional view of an electronic display according to another embodiment of the present invention.

FIG. 6C shows a diagrammatic cross-sectional view of an electronic display according to a further embodiment of the present invention.

FIG. 6D shows a diagrammatic cross-sectional view of an electronic display according to yet another embodiment of the present invention.

Detailed Description

It is generally preferred to have as large as possible of a time-average voltage across the pixel. Methods of maintaining the addressed voltage drop across a pixel during times when the pixel is not being addressed enable rapid addressing of a display. This is because if the voltage across a pixel is maintained even during the time when the pixel is not being addressed, it continues to evolve optically toward a desired state. Therefore, many rows of pixels in the

display, if not all, continue to evolve in parallel when the applied voltage is significantly held. A display of this sort can be addressed much more quickly than a display where the voltage across rows of pixels had decayed to nearly zero during much of the time of the refresh cycle.

Currently, storage capacitors are used in active-matrix liquid crystal displays in order to increase the voltage holding ratio (VHR) of the pixels. The VHR is the ratio of the voltage drop across a pixel just before the next addressing event divided by the voltage across the pixel just after addressing (both voltages referenced to the front plane voltage, which is taken to be zero in this case). However, there are several distinctions for the use of capacitors in electrophoretic or rotating ball displays. First, the capacitance of a pixel in an electrophoretic display or rotating ball display is typically much smaller than a liquid crystal display of the same pixel area. This is because a pixel in an electrophoretic display or rotating ball display will typically be thicker than a liquid crystal display (which is on the order of five microns) and also the dielectric constant is typically lower than for a liquid crystal.

Secondly, electrophoretic and rotating ball displays are driven to optical states that depend upon the sign of an electric field as opposed to a liquid crystal display where the liquid crystal responds to the square of the applied voltage (and thus is independent of the sign of the voltage). In colloquial terms, the electrophoretic and rotating ball displays are "DC driven" while a liquid crystal display is "AC driven." This also means that it is advantageous to switch the voltage of the front plane of an electrophoretic or rotating ball display and this has to be considered when using a storage capacitor.

Thirdly, the goal of the storage capacitor may be different in the two cases. For a liquid crystal display, the storage capacitor is incorporated so that the voltage across the pixel during the time in which the pixel is not addressed is held close to constant, and this allows for accurate addressing of greyscale states. In the case of electrophoretic displays, the storage capacitor may be incorporated to increase the speed of addressing of the display. The speed of addressing is improved because a storage capacitor maintains voltage across a pixel for a longer time than without the storage capacitor. This means that more rows of pixels can evolve under an electric field than without the storage capacitor. In the ideal situation, the voltage is substantially maintained between row addressing events, so that the optical state across the entire display evolves simultaneously.

The present invention features the use of storage capacitors to enhance the performance of an electrophoretic or rotating ball display. Use of a storage capacitor can greatly reduce the rate of decay of the voltage across the pixel. This increases the time-averaged voltage across the pixel, for everything else remaining equal, and so increases the response speed of the electro-optical material, and perhaps increases the optical contrast between oppositely-addressed states.

In addition, the use of a storage capacitor in a "DC driven" display can also provide an advantage in the system and method by which the display is addressed. For displays such as electrophoretic displays, in which particles must move a specific distance to alter the display state of a pixel, the addressing signal (which is typically a voltage) needs to be impressed upon the pixel for a time commensurate with the traverse time of the particles. For example, if the time needed to move particles in a pixel to turn the pixel from white to black (or the reverse) is of the order of milliseconds (i.e. thousandths of a second), an applied voltage that lasts for a duration measured in units, tens or hundreds of microseconds (i.e. millionths of a second) will in general apply such a small driving impetus to the particles that they will not traverse, and the appearance of the pixel will not change significantly. However, if the driving excitation is applied to a pixel plus a storage capacitor designed so that the electric field is maintained for an extended time across the electrophoretic pixel, the field applied by the capacitor may endure for many milliseconds, even though the excitation pulse of microsecond duration has long since disappeared.

One millisecond is one thousand microseconds. A pulse requiring an interval of 1 microsecond for its application to a capacitor exhausts only $1/1000^{th}$ of the one millisecond time span. One can thus successively address 1000 rows of pixels in a time of the order of one millisecond using one power supply.

One controls the power supply to apply a voltage pulse and enough current to charge the pixel plus the storage capacitor to a desired voltage state, using the well-know relation that charge Q on the capacitor is equal to the voltage V times the capacitance C (and is also equal to the integral of the current i(t) with respect to time), or in the usual terminology of electrical engineering,

$$Q = CV = \int idt$$

In this example, the capacitance, C, equals the sum of the capacitances of the pixel and the storage capacitor.

A storage capacitor is a capacitor formed or defined between the pixel electrode and another electrode in the active matrix panel. The pixel electrode will be referred to as the transistor pixel electrode, and as the storage capacitor pixel electrode, as the context may require. For example, an areal overlap between the pixel electrode and an adjacent gate line not used to address the pixel under consideration (or an overlap between the pixel electrode and another conductor) can be used to define a storage capacitor. See for example FIG. 1. An insulating material is situated between these overlapping regions of these two conductive elements. This particular embodiment is illustrated in the plan view shown in FIG. 1, in which there are two gate lines 10, 10'. Gate line 10 has a region 12 that overlaps pixel electrode 14. Pixel electrode 14 corresponds to the pixel that is addressed by gate line 10', and not by gate line 10. For completeness, data line 20 is also shown. Other variations are possible.

For example, the pixel electrode 14 could partially overlap a separate conductive element that is tied to a particular voltage. In any case, it is important that the storage capacitance be at least of the order of the capacitance of the pixel, and preferably greater. That way it stores enough charge to significantly prolong the decay in the voltage drop across the pixel. At the top of FIG. 1, there is a second capacitor defined by the overlap of region 12' corresponding to gate line 10' with the partially shown pixel electrode 14'. An additional such capacitor region corresponding to 12' can be understood to be present for each gate line/pixel electrode pair along each data line of the electronic display. The first pixel or the last pixel in a row of pixels may require a separate conductive element, because there is no "next" pixel that requires a gate line. The capacitance of each such capacitor can be controlled by defining the area of overlap (and thus an area A), the thickness of the insulator (and thus the distance d between the conductors) and the material from which the insulator is fabricated (and thus the dielectric constant ε corresponding to the material chosen).

FIG. 2A illustrates a storage capacitor in cross section, showing the insulator 30 between the gate electrode10 and the pixel electrode 14. The value of the storage capacitance, C_s, is given approximately by

$$C_s = \frac{\varepsilon A}{d}$$

where ε is the dielectric constant of the insulator, A is the overlapping area of the electrodes, and d is the distance between the conductors. In order to achieve a relatively large capacitance it is advantageous to use a thin insulating layer between the overlapping electrodes that make up the storage capacitor, thereby making the distance d small. Other choices that will tend to increase the capacitance are to increase the dielectric constant of the insulator, and to form a capacitor with a larger area A. However, controlling the thickness d is generally the most convenient way to control the capacitance.

There are several ways of creating the storage capacitor. In FIG. 2B, one particularly convenient embodiment is shown in part. One can use the same dielectric (or insulator) layer 30 used in construction of the thin-film transistor as the dielectric in the storage capacitor. The pixel electrode 14 and gate electrode 10 are again shown.

Construction of such a capacitor involves depositing the gate lines 10, 10', then an unpatterned dielectric layer 30. Then, a patterned semiconductor layer 40 and data lines and pixel electrodes 14 are deposited to complete the thin film transistor. Also, the design includes an overlap 12 between the pixel electrode 14 and the adjacent gate line 10 not used to address the pixel in order to form the storage capacitor. The advantage of this design is that the dielectric layer 30 need not be patterned, but serves both as the insulator for the thin film transistor and for the storage capacitor.

FIG. 2C depicts an embodiment in which it is desirable to not pattern the semiconductor or semiconductor contact material 40 as well. One could envision a storage capacitor made from the overlap between a pixel electrode 14 and an adjacent gate line 10 as detailed earlier, and with both the insulator 30 and active semiconductor layer 40 in between. In this scheme, one would have to make sure that leakage through the semiconductor layer 40 does not cause undesirable cross-talk between electrical components.

In another scheme, a separate insulator could be patterned over the lower electrode of the storage capacitor, then the pixel electrode overlaps over that region, thus forming the storage capacitor.

FIG. 2D shows an embodiment in which the insulator 30 is situated between the pixel electrode 14 and another conductor 16, which can for example be connected to the same voltage as the front electrode of the display, which conductor 16 overlaps with pixel electrode 14 over an area A.

FIG. 3 illustrates the lumped circuit diagrams for two variations of the use of a storage capacitor. In one embodiment, shown in FIG. 3A, the storage capacitor 92' is tied to an adjacent gate line 10 that is not used to address the pixel under consideration, as described earlier. In another embodiment shown in FIG. 3B, the capacitor 92' is tied to a separate conductive line 16 preferably tied to a voltage that follows the front-plane voltage. The pixel 35 is represented as a parallel resistor and capacitor tied to V_{com}, which is the voltage of the front plane. Although this is by no means a complete model, it is useful to demonstrate the advantage of a storage capacitor. If a voltage is applied to the pixel at zero time then the transistor is brought quickly into depletion so that its resistance can be taken to be infinite (for ease of calculation), then the voltage on the pixel decays exponentially. If there were no storage capacitor, the characteristic decay time, the time span over which the voltage decays to 1/e of its initial value, is given by the RC time constant, or R_pC_p. Adding the storage capacitor having capacitance C_s increases the voltage decay time to approximately $R_p(C_p+C_s)$.

An exemplary embodiment of a thin-film transistor and a thin film capacitor for use in an encapsulated electrophoretic display is shown in FIG. 4A in plan view. Referring to FIG. 4A, this exemplary embodiment includes data lines 30', 32', a selection line 36', a pixel electrode 34', and a capacitor 92'. Various physical dimensions are indicated, in microns.

The embodiment of FIG. 4A is illustrated in cross section in FIG. 4B, though not to scale. Referring to FIG. 4B, the embodiment includes gate electrodes 53', a dielectric layer 54' which can be SiN or another dielectric material, a semiconductor layer 56' which can be amorphous silicon or another semiconductor material, semiconductor contacts 58', which can be made from amorphous silicon or another semiconductor material, to the drain and pixel electrodes 59'. Capacitor 92' is shown in this exemplary embodiment also with dielectric layer 54', semiconductor layer 56', semiconductor contact 58' and an electrode layer.

To illustrate the operating characteristics of the embodiment of FIG. 4A and 4B, samples were prepared through either a two-mask process, as preferred, or a three-mask process, for

comparison. In the two-mask process, the SiN dielectric layer 54' and the amorphous silicon layer 56' were not patterned while in the three mask process both the SiN dielectric layer 54' and the amorphous silicon layer 56' were patterned. The physical and experimentally measured electrical characteristics for these two samples are given in Table I.

Table I

Sample	W/L	On/Off Ratio	Mobility	Threshold Voltage	G_m	Max. Drain Current	Min. Drain Current	Storage capacitance
Patterned	200/20	$1x10^8$	$.55cm^2/Vs$	5.0V	$18.9nA/V^2$	10μA	0.1pA	19.1 pF
Unpatterned	160/20	$3.3x10^5$	$.43cm^2/Vs$	5.0V	$23.4nA/V^2$	20μA	60pA	18.4 pF

The leakage current and On/Off ratio for the unpatterned sample, as expected, are poorer than for the patterned sample. The unpatterned sample, however, is both suitable and preferable for many display applications. Referring to FIG. 5, the drain current versus gate voltage characteristics of the two-mask sample are shown. The drain current can be caused to vary by over five orders of magnitude by changing the gate voltage from zero to 30 volts. This large range makes this transistor suitable for many display applications. Further alternative embodiments of a thin-film transistor array can be employed, as will be recognized by those of ordinary skill in the electronic display arts.

As mentioned before, the display can be an electrophoretic display. Electrophoretic displays have been the subject of intense research and development for a number of years. Electrophoretic displays have attributes of good brightness and contrast, wide viewing angles, state bistability, and low power consumption when compared with liquid crystal displays. Nevertheless, problems with the long-term image quality of these displays have prevented their widespread usage. For example, particles that make up such displays tend to cluster and settle, resulting in inadequate service-life for these displays.

An encapsulated, electrophoretic display typically does not suffer from the clustering and settling failure mode of traditional electrophoretic devices and provides further advantages, such as the ability to print or coat the display on a wide variety of flexible and rigid substrates. Use of the word "printing" is intended to include all forms of printing and coating, including, but

without limitation: premetered coatings such as patch die coating, slot or extrusion coating, slide or cascade coating, and curtain coating; roll coating such as knife over roll coating, forward and reverse roll coating; gravure coating; dip coating; spray coating; meniscus coating; spin coating; brush coating; air knife coating; silk screen printing processes; electrostatic printing processes; thermal printing processes; and other similar techniques. Thus, the resulting display can be flexible. Further, because the display media can be printed (using a variety of methods), the display itself can be made inexpensively.

In broad overview, the invention relates to encapsulated electrophoretic displays that provide a flexible, reflective display that can be manufactured easily and consume little power (or no power in the case of bistable displays in certain states), as well as materials and methods useful in their construction. Such displays, therefore, can be incorporated into a variety of applications. The display can be formed from and can include particles that move in response to an electric charge. This mode of operation is typical in the field of electrophoretics. A display in which the particles, ordered by an electric charge, take on a certain configuration can take on many forms. Once the electric field is removed, the particles can be generally stable (*e.g.*, bistable). Additionally, providing a subsequent electric charge can alter a prior configuration of particles. Some encapsulated electrophoretic displays may include two or more different types of particles. Such displays may include, for example, displays containing a plurality of anisotropic particles and a plurality of second particles in a suspending fluid. Application of a first electric field may cause the anisotropic particles to assume a specific orientation and present an optical property. Application of a second electric field may then cause the plurality of second particles to translate, thereby disorienting the anisotropic particles and disturbing the optical property. Alternatively, the orientation of the anisotropic particles may allow easier translation of the plurality of second particles. The particles may have a refractive index that substantially matches the refractive index of the suspending fluid.

An encapsulated electrophoretic display can be constructed so that the optical state of the display is stable for some length of time. When the display has two states that are stable in this manner, the display is bistable. If more than two states of the display are stable, then the display is multistable. For the purpose of the present invention, the term bistable indicates a display in which any optical state remains fixed once the addressing voltage is removed. However, the definition of a bistable state depends upon the display's application. A slowly decaying optical

state can be effectively bistable if the optical state is substantially unchanged over the required viewing time. For example, in a display that is updated every few minutes, a display image that is stable for hours or days is effectively bistable for a particular application. Thus, for purposes of the present invention, the term bistable also indicates a display with an optical state sufficiently long-lived so as to be effectively bistable for a particular application. Alternatively, it is possible to construct encapsulated electrophoretic displays in which the image decays quickly once the addressing voltage to the display is removed (*i.e.*, the display is not bistable or multistable). Whether or not an encapsulated electrophoretic display is bistable, and its degree of bistability, can be controlled through appropriate chemical modification of the electrophoretic particles, the suspending fluid, the capsule, and binder materials.

An encapsulated electrophoretic display may take many forms. The display may include capsules dispersed in a binder. The capsules may be of any size or shape. The capsules may, for example, be spherical and may have diameters in the millimeter range or the micron range, but are preferably from about ten to about a few hundred microns. The capsules may be formed by an encapsulation technique. Particles may be encapsulated in the capsules. The particles may be two or more different types of particles. The particles may be colored, luminescent, light-absorbing or transparent, for example. The particles may include neat pigments, dyed (laked) pigments or pigment/polymer composites, for example. The display may further include a suspending fluid in which the particles are dispersed.

Generally, an encapsulated electrophoretic display includes a capsule with one or more species of particle that either absorb or scatter light and that are suspended in a fluid. One example is a system in which the capsules contain one or more species of electrophoretically mobile particles dispersed in a dyed suspending fluid. Another example is a system in which the capsules contain two separate species of particles suspended in a clear suspending fluid, in which one species of particle absorbs light (black), while the other species of particle scatters light (white). There are other extensions (more than two species of particles, with or without a dye, *etc.*). The particles are commonly solid pigments, dyed particles, or pigment/polymer composites.

In electrophoretic displays, the particles may be oriented or translated by placing an electric field across the capsule. The electric field may include an alternating-current field or a

direct-current field. The electric field may be provided by at least one pair of electrodes disposed adjacent to a display comprising the capsule.

The successful construction of an encapsulated electrophoretic display requires the proper interaction of all these materials and processes. Materials such as a polymeric binder (for example, for binding the capsules to a substrate), electrophoretic particles, fluid (for example, to surround the electrophoretic particles and provide a medium for migration), and a capsule membrane (for example, for enclosing the electrophoretic particles and fluid) must all be chemically compatible. The capsule membranes may engage in useful surface interactions with the electrophoretic particles, or may act as an inert physical boundary between the fluid and the binder. Polymer binders may set as adhesives between capsule membranes and electrode surfaces.

Materials for use in creating electrophoretic displays relate to the types of materials, including, but not limited to, particles, dyes, suspending fluids, and binders used in fabricating the displays. In one embodiment, types of particles that may be used to fabricate suspended particle displays include scattering pigments, absorbing pigments and luminescent particles. Such particles may also be transparent. Exemplary particles include titania, which may be coated in one or two layers with a metal oxide, such as aluminum oxide or silicon oxide, for example. Such particles may be constructed as corner cubes. Luminescent particles may include, for example, zinc sulfide particles. The zinc sulfide particles may also be encapsulated with an insulative coating to reduce electrical conduction. Light-blocking or absorbing particles may include, for example, dyes or pigments. Types of dyes for use in electrophoretic displays are commonly known in the art. Useful dyes are typically soluble in the suspending fluid, and may further be part of a polymeric chain. Dyes may be polymerized by thermal, photochemical, and chemical diffusion processes. Single dyes or mixtures of dyes may also be used.

A suspending (*i.e.*, electrophoretic) fluid may be a high resistivity fluid. The suspending fluid may be a single fluid, or it may be a mixture of two or more fluids. The suspending fluid, whether a single fluid or a mixture of fluids, may have its density substantially matched to that of the particles within the capsule. The suspending fluid may be halogenated hydrocarbon, such as tetrachloroethylene, for example. The halogenated hydrocarbon may also be a low molecular

weight polymer. One such low molecular weight polymer is poly(chlorotrifluoroethylene). The degree of polymerization for this polymer may be from about 2 to about 10.

Furthermore, capsules may be formed in, or later dispersed in, a binder. Materials for use as binders include water-soluble polymers, water-dispersed polymers, oil-soluble polymers, thermoset polymers, thermoplastic polymers, and uv- or radiation-cured polymers.

In some cases, a separate encapsulation step of the process is not necessary. The electrophoretic fluid may be directly dispersed or emulsified into the binder (or a precursor to the binder material) to form what may be called a "polymer-dispersed electrophoretic display." In such displays, the individual electrophoretic phases may be referred to as capsules or microcapsules even though no capsule membrane is present. Such polymer-dispersed electrophoretic displays are considered to be subsets of encapsulated electrophoretic displays.

In an encapsulated electrophoretic display, the binder material surrounds the capsules and separates the two bounding electrodes. This binder material must be compatible with the capsule and bounding electrodes and must possess properties that allow for facile printing or coating. It may also possess barrier properties for water, oxygen, ultraviolet light, the electrophoretic fluid, or other materials, Further, it may contain surfactants and cross-linking agents, which could aid in coating or durability. The polymer-dispersed electrophoretic display may be of the emulsion or phase separation type.

Referring to FIG. 6A, an embodiment of an electrophoretic display that employs a thin-film transistor array of the present invention is shown. FIG. 6A shows a diagrammatic cross-section of an electrophoretic display 130 constructed using electronic ink. The binder 132 includes at least one capsule 134, which is filled with a plurality of particles 136 and a dyed suspending fluid 138. In one embodiment, the particles 136 are titania particles. When a direct-current electric field of the appropriate polarity is applied across the capsule 134, the particles 136 move to the viewed surface of the display and scatter light. When the applied electric field is reversed, the particles 136 move to the rear surface of the display and the viewed surface of the display then appears dark.

FIG. 6B shows a cross-section of another electrophoretic display 140 constructed using electronic ink. This display comprises a first set of particles 142 and a second set of particles 144 in a capsule 141. The first set of particles 142 and the second set of particles 144 have

contrasting optical properties. For example, the first set of particles 142 and the second set of particles 144 can have differing electrophoretic mobilities. In addition, the first set of particles 142 and the second set of particles 144 can have contrasting colors. For example, the first set of particles 142 can be white, while the second set of particles 144 can be black. The capsule 141 further includes a substantially clear fluid. The capsule 141 has electrodes 146 and 146' disposed adjacent it. The electrodes 146, 146' are connected to a source of voltage 148, which may provide an electric field to the capsule 141. In one embodiment, upon application of an electric field across the electrodes 146, 146', the first set of particles 142 move toward electrode 146', while the second set of particles 144 move toward electrode 146. In another embodiment, upon application of an electric field across the electrodes 146, 146', the first set of particles 142 move rapidly toward electrode 146', while the second set of particles 144 move only slowly or not at all towards electrode 146, so that the first set of particles packs preferentially at the microcapsule surface adjacent to electrode 146'.

FIG. 6C shows a diagrammatic cross-section of a suspended particle display 150. The suspended particle display 150 includes needle-like particles 152 in a transparent fluid 154. The particles 152 change their orientation upon application of an AC field across the electrodes 156, 156'. When the AC field is applied, the particles 152 are oriented perpendicular with respect to the display surface and the display appears transparent. When the AC field is removed, the particles 152 are randomly oriented and the display 150 appears opaque.

The electrophoretic and suspended particle displays provided in FIGS. 6A-6C are exemplary only, and other electrophoretic displays can be used in accordance with the present invention.

In another detailed embodiment, the display medium 106 can comprise a plurality of bichromal spheres shown in FIG. 6D. A bichromal sphere 160 typically comprises a positively charged hemisphere 162 of a first color and a negatively charged hemisphere 164 of a second color in a liquid medium 166. Upon application of an electric field across the sphere 160 through a pair of electrodes 168, 168', the sphere 160 rotates and displays the color of one of the two hemispheres 162, 164.

Equivalents

While the invention has been particularly shown and described with reference to specific preferred embodiments, it should be understood by those skilled in the art that various changes in

form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

Claims

1. An electronic display comprising:

an encapsulated display medium comprising a plurality of pixels;

a transistor having a data electrode, a gate electrode and a pixel electrode and comprising a layer of insulating material situated between a first layer of conductive material that forms the gate electrode and a second layer of conductive material that forms the data and pixel electrodes, the transistor applying an addressing voltage to one of the pixels via the transistor pixel electrode; and

a storage capacitor comprising a layer of insulating material situated between a first layer of conductive material and a second layer of conductive material, said storage capacitor in electrical communication with the pixel addressed by the transistor for reducing a rate of voltage decay across the pixel.

2. The display of claim 1 wherein each of said pixels comprises an electrophoretic display medium comprising at least one capsule containing particles disposed in a fluid.

3. The display of claim 1 wherein one of said layers of material comprising said transistor and a respective layer of material comprising said storage capacitor comprise a continuous layer of material.

4. The display of claim 1 wherein said transistor and said storage capacitor each further comprise a layer of semiconducting material situated between said respective first layers of conductive material and said respective second layers of conductive material.

5. The display of claim 4 wherein one of said layers of material comprising said transistor and a respective layer of material comprising said storage capacitor comprise a continuous layer of material.

6. The display of claim 4 wherein said transistor and said storage capacitor comprise a plurality of continuous layers of material.

7. The display of claim 1 wherein the storage capacitor is in electrical communication with a second gate line different from a first gate line in electrical communication with the transistor gate electrode for addressing the pixel.

8. The display of claim 1 wherein the storage capacitor is in electrical communication with a conductor.

9. The display of claim 1 wherein the storage capacitor comprises a storage capacitor pixel electrode, an insulator disposed adjacent the pixel electrode and a storage capacitor gate electrode disposed adjacent the insulator.

10. The display of claim 9 wherein the insulator is patterned.

11. The display of claim 9 wherein the insulator is unpatterned.

12. The display of claim 9 wherein the insulator forms a part of the storage capacitor and the transistor.

13. The display of claim 1 wherein the storage capacitor comprises a storage capacitor pixel electrode, a semiconductor layer disposed adjacent the storage capacitor pixel electrode, an insulator layer disposed adjacent the semiconductor, and a storage capacitor gate electrode disposed adjacent the insulator.

14. The display of claim 1 wherein the storage capacitor comprises a storage capacitor pixel electrode, an insulator disposed adjacent the storage capacitor pixel electrode and a conductor disposed adjacent the insulator.

15. The display of claim 1 wherein a capacitance of the storage capacitor is greater than a capacitance of the pixel.

16. The display of claim 1 wherein a voltage decay time across the pixel is based on the product of R_p and $(C_p + C_s)$ where R_p is a resistance of the pixel, C_p is a capacitance of the pixel, and C_s is a capacitance of the storage capacitor.

17. The display of claim 1 wherein said transistor and said storage capacitor comprise a plurality of continuous layers of material.

18. An electronic display comprising:

an encapsulated electrophoretic display medium comprising a plurality of pixels; and

a storage capacitor comprising a layer of insulating material situated between a first layer of conductive material and a second layer of conductive material, said storage capacitor in

electrical communication with one of said plurality of pixels for reducing a rate of voltage decay across the pixel.

19. A method of addressing an electronic display having a display medium comprising a plurality of pixels and a plurality of storage capacitors, at least one of said plurality of storage capacitors in electrical communication with a corresponding one of said plurality of pixels, the method comprising:

applying an electric pulse to the pixel and storage capacitor to charge the pixel and storage capacitor to an addressing voltage, the duration of the electric pulse being insufficient in length to fully address the pixel directly, so that the pixel is addressed and presents an intended appearance after the electric pulse ends.

20. The method of claim 19 wherein a plurality of electric pulses are successively applied to a plurality of pixels and storage capacitors, each pulse charging the respective pixel and storage capacitor to an addressing voltage of the corresponding pixel, an individual duration of an electric pulse being insufficient in length to fully address a pixel directly, so that the pixels are addressed and present an intended image after the electric pulses end.

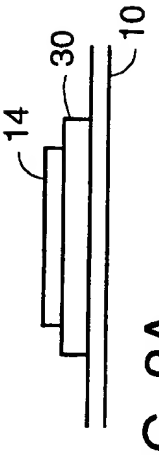

FIG. 2A

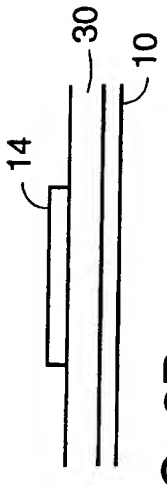

FIG. 2B

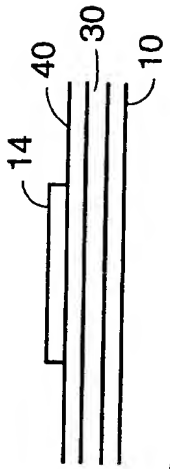

FIG. 2C

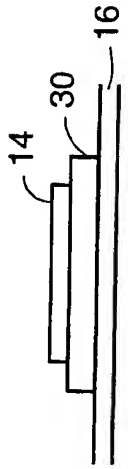

FIG. 2D

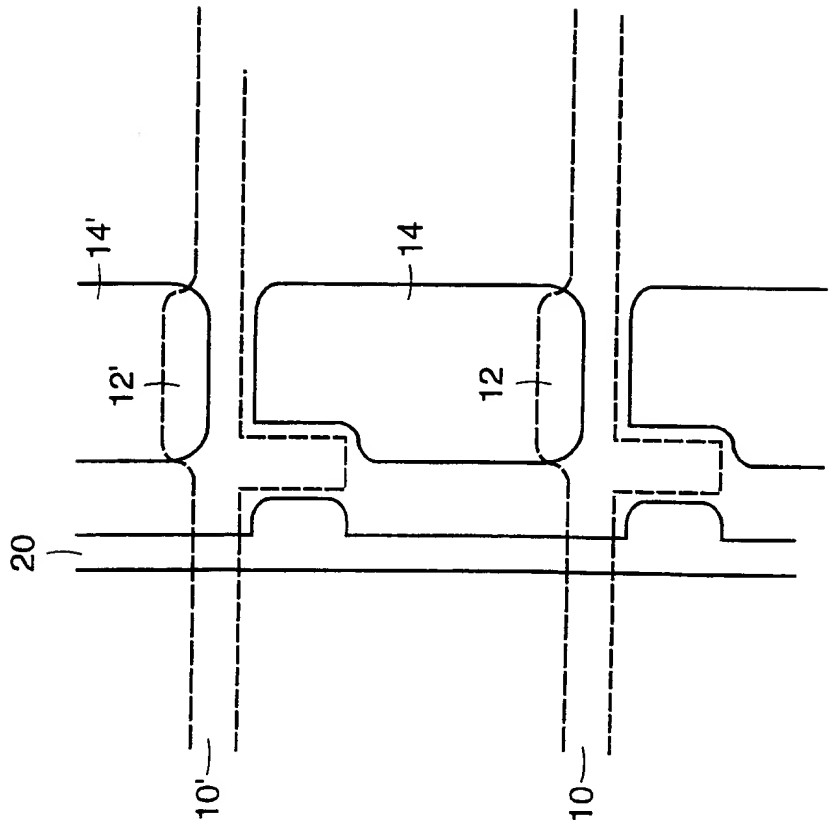

FIG. 1

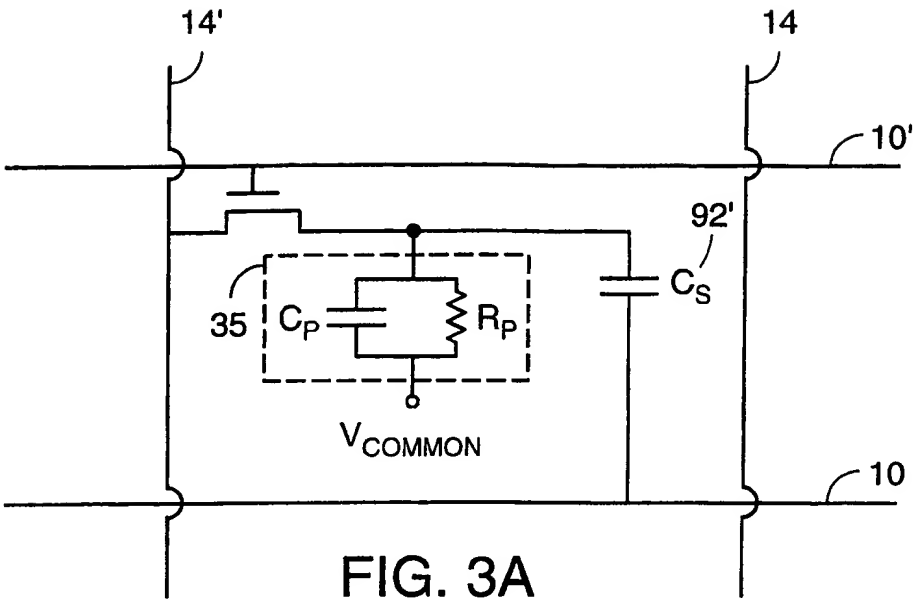
14'
14
10'
92'
C_S
35
C_P
R_P
V_{COMMON}
10

FIG. 3A

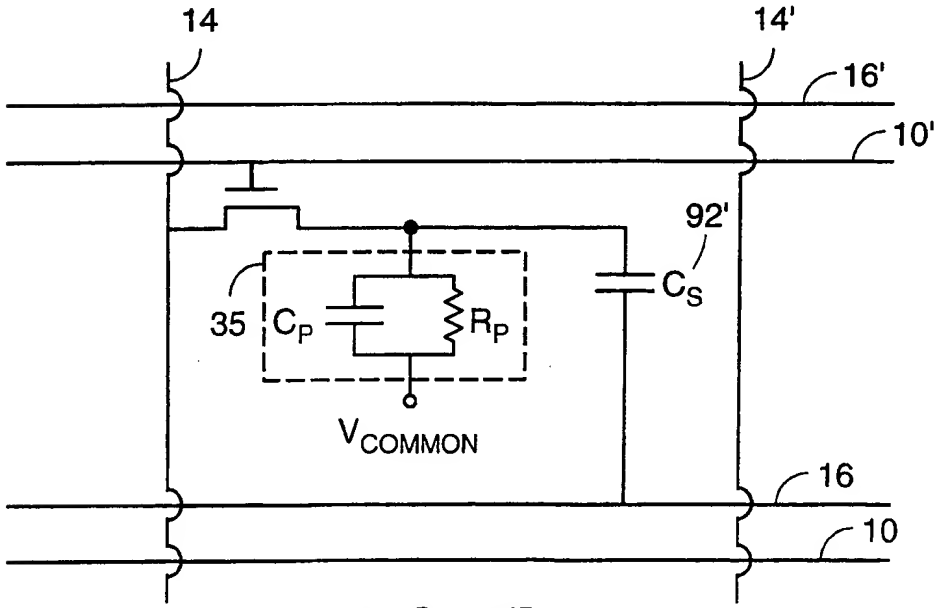
14
14'
16'
10'
92'
C_S
35
C_P
R_P
V_{COMMON}
16
10

FIG. 3B

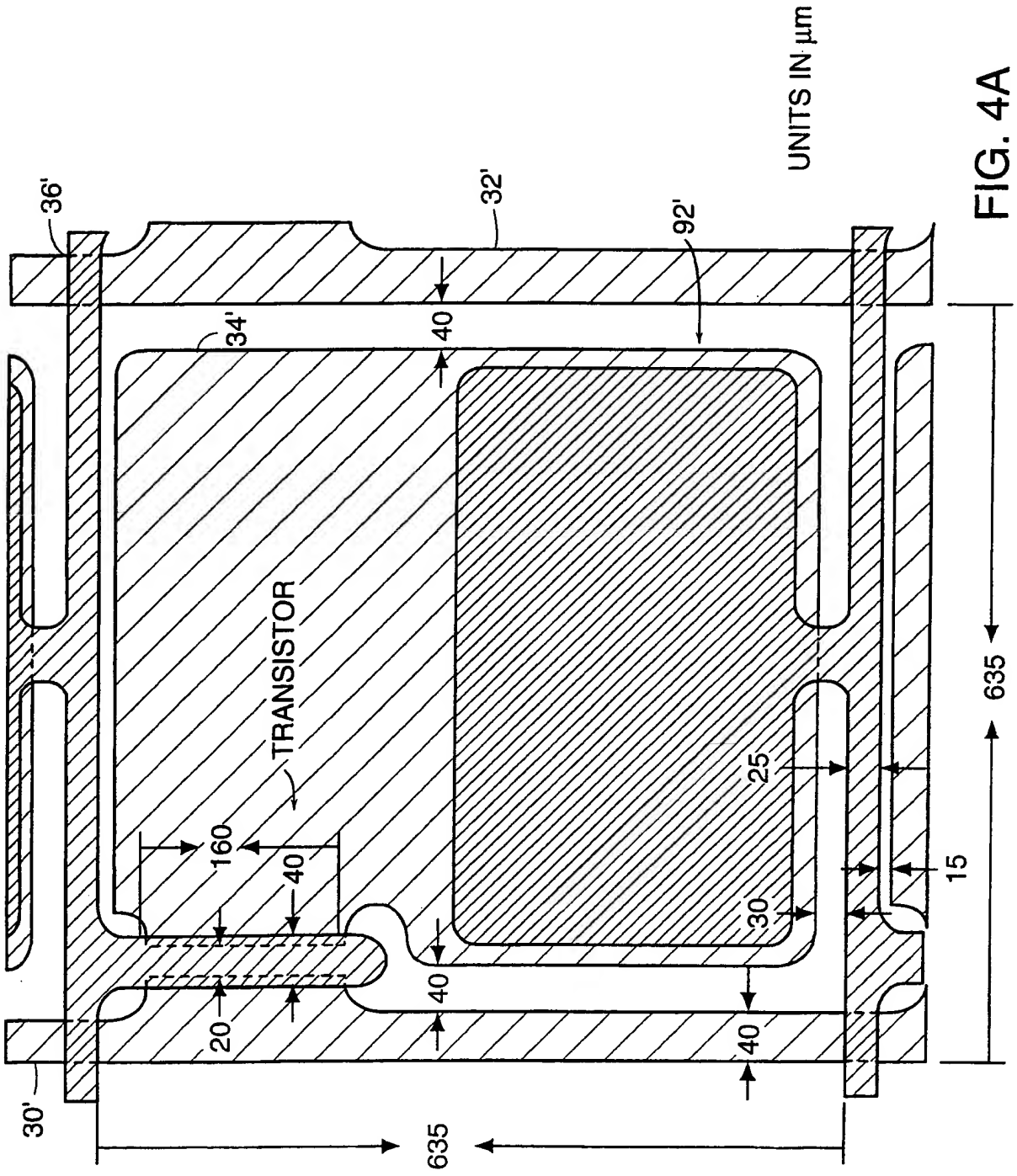
UNITS IN µm
36'
32'
92'
34'
40
TRANSISTOR
160
40
25
30
15
635
20
40
40
30'
635

FIG. 4A

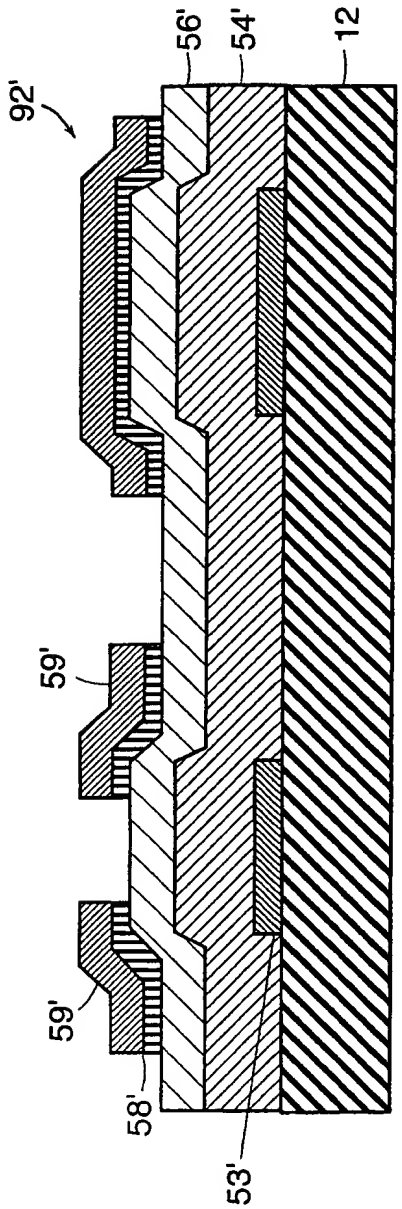

FIG. 4B

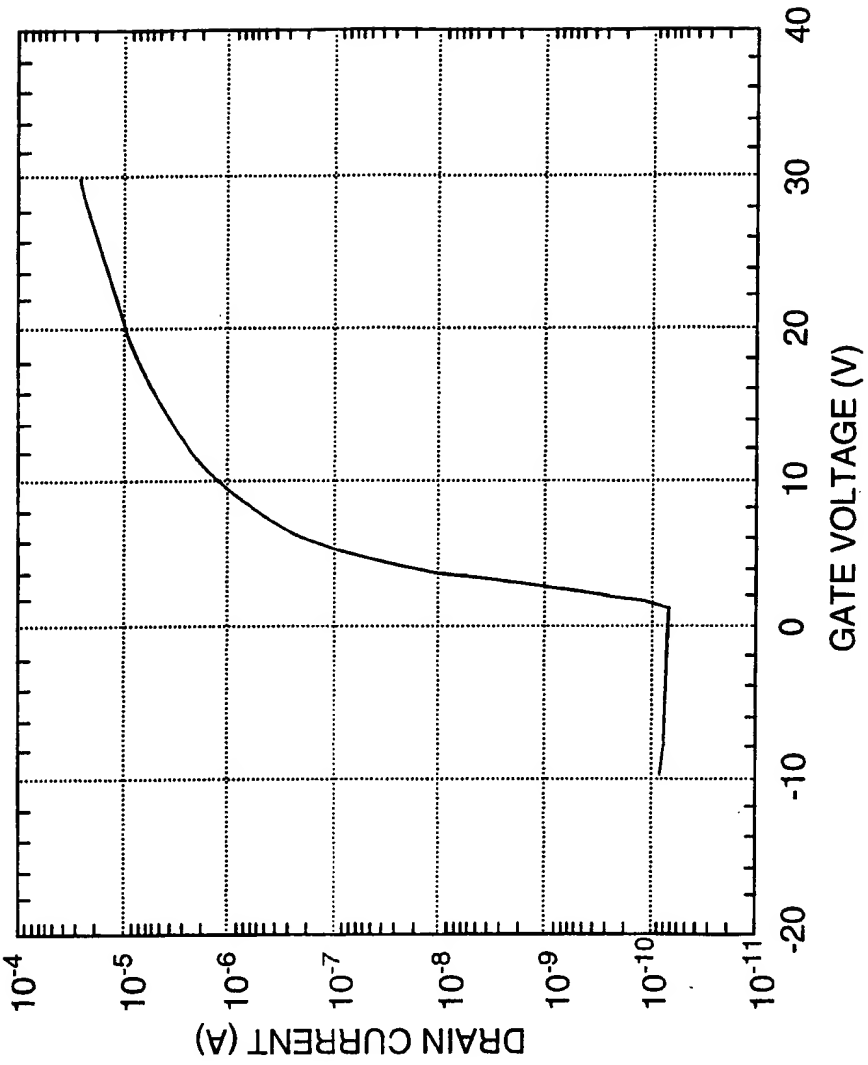
DRAIN CURRENT (A)
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
GATE VOLTAGE (V)
-20
-10
0
10
20
30
40

FIG. 5

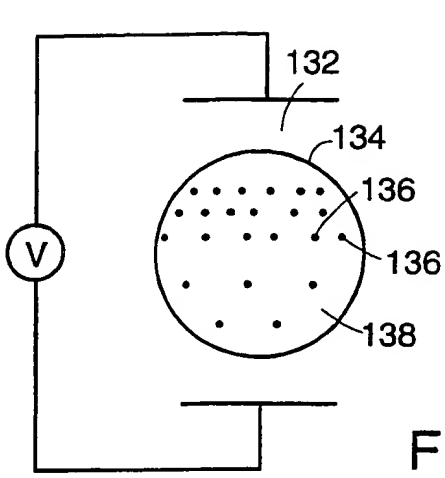

FIG. 6A

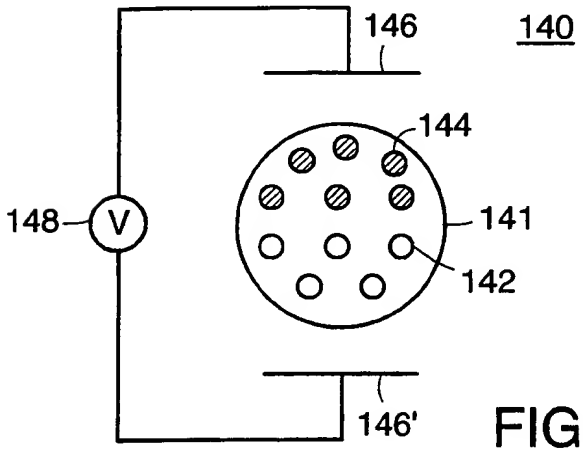

FIG. 6B

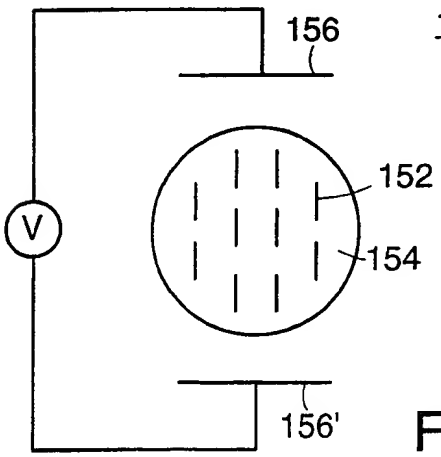

FIG. 6C

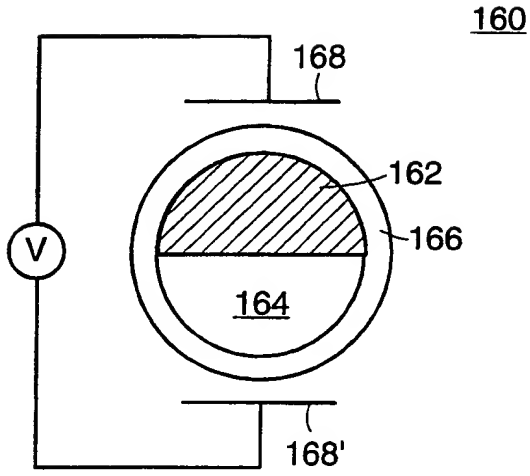

FIG. 6D

INTERNATIONAL SEARCH REPORT

Internati . Application No
PCT/US 00/19997

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G02F1/1362

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G02F H01L G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 641 974 A (DEN BOER WILLEM ET AL) 24 June 1997 (1997-06-24) column 4, line 31 - line 60 column 6, line 25 - line 55; claims 1,2; figure 1 ---	1,3-20
A	EP 0 717 446 A (EASTMAN KODAK CO) 19 June 1996 (1996-06-19) page 5, line 9 - line 42; figure 1 ---	1,3-20
A	US 5 238 861 A (CONTELLEC MICHEL LE ET AL) 24 August 1993 (1993-08-24) column 2, line 10 -column 3, line 13 column 5, line 10 - line 40; figures 3,13 abstract --- -/--	1,3-20

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 November 2000	04/12/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Manntz, W

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Internat. .l Application No
PCT/US 00/19997

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,A	WO 99 42983 A (BURROUGHES JEREMY HENLEY ;CAMBRIDGE DISPLAY TECH (GB); FRIEND RICH) 26 August 1999 (1999-08-26) page 1, paragraph 5 -page 2, paragraph 2 page 8, paragraph 1 - paragraph 2; figure 1 ---	1,3-20
A	PATENT ABSTRACTS OF JAPAN vol. 013, no. 316 (P-900), 18 July 1989 (1989-07-18) & JP 01 086116 A (NIPPON MEKTRON LTD), 30 March 1989 (1989-03-30) abstract -----	2

INTERNATIONAL SEARCH REPORT

Information on patent family members

Internat ..l Application No
PCT/US 00/19997

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